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DVR OPTIMIZATION TECHNIQUE FOR 3-PHASE PHASE-CONTROLLED RECTIFIER*

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Abstract: This paper proposes optimization technique and analytical analysis for the response time of DVR (Dynamic Voltage Restorer). We analyze the possible compensation range of voltage dip by the DVR system using proposed optimization technique for the response time. To protect 3-phase phase-controlled rectifier (PCR) from voltage dip, DVR system needs to have optimum response time as an important design factor. Although the fast response time of DVR ensures wider range of voltage dip, DVR controller has so high cost and poor stability. In this paper, we also presents optimum response time required for certain intensity of voltage dips for the DVR system, and good stability to support possible compensation range of voltage dip. The proposed technique showed optimum response time and good stability for overall system.

Key words: *DVR, response time, voltage dip, 3-phase phase-controlled rectifier (PCR)*

Mathematics Subject Classification: *65G20, 65Y10*

1 Introduction

Voltage dip is a momentary voltage reduction phenomenon of over 20% for 0.05∼0.1 seconds, and it is mostly caused by incidental accidents such as short circuit and over current. The voltage dip primarily causes fatal malfunction of control unit and commutation failure on switching element kept at large-scale plants that use inverter, resulting in overall system failure [1, 2]. The problems caused by voltage dip are especially severe in SCR (Silicon-Controlled Rectifier) converter and inverter [3]. Recently, DVR (Dynamic Voltage Restorer) has been utilized as an alternative solution for voltage dip that causes severe damages for rolling process stage at iron mills and semiconductor factories. Unlike UPS (Uninterrupted Power Supply) that compensates for total capacity of load, DVR only compensates the reduced voltage, DVR can be used as an alternative countermeasure for voltage dip at large load capacities where UPS cannot be installed. Thus, DVR has become important issue as a solution for voltage dip which falls under the most categories of power failure, and many researches have studied on DVR [4-8].

Choi et al. [4] suggested a method to minimize compensation energy by setting the effective power supply provided by DVR at 0, and Zhan et al. [5] designed phase-locked loop to detect the optimal phase angle from unbalanced power source. Choi et al. [6] also suggested a method to design the required filter that is acceptable for DVR inverter output,

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while Fitzer et al. [7] made use of state space matrix to suggest a method for faster detection of voltage dip. Vilathgamuwa et al. [8] used multi-loop feedback controller to improve the compensation range at variable loads.

Although many researchers have studied on DVR, no researchers have been done to find out the range of voltage dip that can be compensated by the DVR at specific system. ITIC [9] used CBEMA curve to suggest the possible range and occurrence time of voltage dip for various electrical devices, while Bollen et al. [10] researched on permissible range, phase and duration of voltage dip for DVR. However, it only suggested the estimated range of voltage dip for ordinary electrical devices and systems.

This paper analyzes the relationship between possible compensation range of voltage dip, and the response time of DVR as an important design factor to protect 3-phase phase-controlled rectifier (PCR) from voltage dip. We investigate the magnitude and phase range of voltage dip that can be compensated according to the optimum response time of DVR. In this paper, we also present optimization technique for the response time of DVR, and compensation technique of voltage dip of DVR using optimum response time.

2 Basic Theory and Analytical Analysis

2.1 Commutation Failure Analysis for the Voltage Dip

Phase-controlled rectifier (PCR) as a power converter uses SCR to convert AC power into variable DC power, and the switching "ON" time of SCR can be changed to adjust the level of DC output.

Let's explain the operation state and the waveform of 3-phase PCR for the commutation failure analysis using operation principles of 3-phase PCR described in previous research [1]. Since PCR can basically operate in both rectification mode and inverter mode, it is possible to restore the regeneration power that is produced during deceleration of electric motor connected to the loading side. L_s represents inductance of power line due to the effect of transformer, and because this inductance limits sudden changes in the current passing through line voltage, the current overlapping phenomenon occurs. The parameter α represents firing angle, α_1 represents overlapping interval, and α_2 represents SCR's turn-off time. From the condition where the T_1 and T_2 are turn-on, and then if T_3 is turn-on, the inverse voltage v_{ba} is applied to T_1. Therefore i_a decrease gradually and i_b increase from 0[A]. If i_a decreases from I_0[A] to 0[A], the current commutation is terminated and T_1 is turn-off. However, in order for T_1 to be completely turn-off, the current must be terminated before $(\pi - \alpha_2)$. In other words, once i_a becomes 0[A], reverse bias voltage at T_1 greater than α_2 must be sent to completely turn T_1 off . If it is not terminated before $(\pi - \alpha_2)$, turn-off time at T_1 cannot be followed which prevents complete turn-off state, and when this happens, it will be turn-on again to cause commutation failure if forward bias voltage is sent to T_1. If commutation failure is observed at T_1 and it is not completely turn-off, T_1, T_2 and T_3 are maintained at "ON" state, and when the next trigger signal is sent to T_4 allowing T_4 to be turn-on, the short circuit is produced between T_1 and T_4, which destroys PCR, which may cause severe damages to the entire system.

2.2 Commutation Failure for the 3-Phase Parallel Voltage Dip

Now let's analyze the range of voltage dip that causes commutation failure on 3-phase PCR. Identical voltage dip may have different effects on commutation failure depending on operation state of the PCR, so the worst case that can cause commutation failure is

assumed. Let's assume that voltage dip occurs as soon as trigger signal is sent to each PCR, and voltage dip is maintained for more than 1 period to extract a condition where shortest voltage dip time may cause commutation failure. This period is enough to cause commutation failure.

Although most of voltage dips are known to be single phase voltage dip [3], we analyze voltage dip occurring at 3 phases at the same time and voltage dip occurring at single phase to extract more reliable and worst scenarios.

Let's investigate the range of voltage dip that can cause commutation failure in 3-phase PCR, and it is assumed that equal voltage dip occurs on all 3 phases.

Input voltages of 3 phases are defined as follows:

$$v_a(t) = \sqrt{2}V_m \cos\left(\omega t + \frac{\pi}{3}\right) \tag{2.1}$$

$$v_b(t) = \sqrt{2}V_m \cos\left(\omega t - \frac{\pi}{3}\right) \tag{2.2}$$

$$v_c(t) = \sqrt{2}V_m \cos\left(\omega t + \pi\right) \tag{2.3}$$

where, the V_m represents effective phase voltage of input signal, and ω represents angular velocity. If line voltages, (2.1)$\sim$(2.3) are used when identical voltage dip occurs on all 3 phases, it can be expressed as follows:

$$v_{a-dip}(t) = \sqrt{2}V_{dip} \cos\left(\omega t + \frac{\pi}{3} + \phi\right) \tag{2.4}$$

$$v_{b-dip}(t) = \sqrt{2}V_{dip} \cos\left(\omega t - \frac{\pi}{3} + \phi\right) \tag{2.5}$$

$$v_{c-dip}(t) = \sqrt{2}V_{dip} \cos\left(\omega t + \pi + \phi\right) \tag{2.6}$$

where V_{dip} represents effective value of voltage dip, and ϕ represents change in phase during the voltage dip. If voltage dip occurs when trigger signal is applied at T_3, commutation failure may generate reverse bias voltage at T_1 , and reverse bias voltage at T_1 can be expressed as:

$$v_{ba-dip}(t) = \sqrt{6}V_{dip} \sin\left(\omega t + \phi\right) \tag{2.7}$$

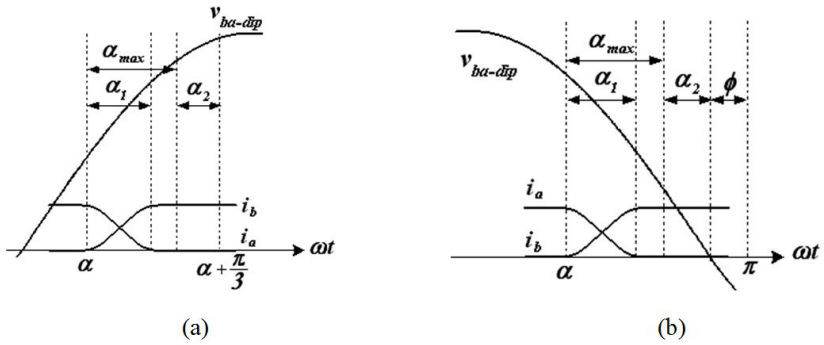

Figure 1: Voltage and current according to the firing angle for the commutation: (a) $\alpha \leq \left(\frac{2\pi}{3} - \phi\right)$, (b) $\alpha > \left(\frac{2\pi}{3} - \phi\right)$

Fig. 1 shows voltage and current waveforms for commutation region, and waveforms are divided into 2 sections depending on the position of firing angle. If firing angle is larger

than $(2\pi/3-\phi)$, the applied voltage v_{ba} at T_1 only provides reverse bias voltage of up to $(\pi-\phi)$, thus T_1 must be completely turn-off before $(\pi-\phi)$. If T_1 is not turn-off before that time, it will be turn-on as soon as forward voltage is applied after $(\pi-\phi)$, and it will cause commutation failure. If firing angle is no larger than $(2\pi/3-\phi)$, T_1 must be completely turn-off before the next trigger signal is sent to T_4. Although the value of overlap angle, α_1 may change the size of voltage dip, the current must be terminated before the maximum acceptable overlap angle $\alpha_{\max}$ to avoid commutation failure. From Fig. 1, the condition that will cause commutation failure can be expressed as:

$$\alpha \le \left(\frac{2\pi}{3}-\phi\right) : \int_{\alpha}^{\pi+60^\circ-\alpha_2} v_{ba,dip}(t)d\omega t < 2\omega L_s I_o \tag{2.8}$$

$$\alpha > \left(\frac{2\pi}{3}-\phi\right) : \int_{\alpha}^{\pi-\phi-\alpha_2} v_{ba,dip}(t)d\omega t < 2\omega L_s I_o \tag{2.9}$$

Substituting (2.7) into Equation (2.8)-(2.9), it is expressed as:

$$\alpha \le \left(\frac{2\pi}{3}-\phi\right) : \sqrt{6}v_{dip}\left[\cos(\alpha+\phi)-\cos\left(\alpha+\frac{\pi}{3}-\alpha_2+\phi\right)\right] < 2\omega L_s I_o \tag{2.10}$$

$$\alpha > \left(\frac{2\pi}{3}-\phi\right) : \sqrt{6}v_{dip}[\cos(\alpha+\phi)-\cos(\pi-\alpha_2)] < 2\omega L_s I_o \tag{2.11}$$

2.3 Commutation Failure for the Single Phase Voltage Dip

Since voltage dip of single phase observed at A phase or B phase may have an effect on commutation failure of SCR T_1, we investigate the single phase voltage dip for A phase and B phase, respectively.

(1) Single Phase Voltage Dip for A Phase

If voltage dip occurs on A phase, the reverse voltage applied at T_1 is shown in Equation (2.12).

$$\begin{aligned} v_{ba-Adip}(t) &= \sqrt{2}V_m\cos\left(\omega t-\frac{\pi}{3}\right)-\sqrt{2}V_{dip}\cos\left(\omega t+\frac{\pi}{3}+\phi\right) \\ &= \sqrt{A^2+B^2}\sin(\omega t+\gamma_A) \end{aligned} \tag{2.12}$$

where, $A = \sqrt{2}\left[V_m\frac{\sqrt{3}}{2}+V_{dip}\sin\left(\frac{\pi}{3}+\phi\right)\right]$, $B = \sqrt{2}\left[\frac{V_m}{2}-V_{dip}\cos\left(\frac{\pi}{3}+\phi\right)\right]$ and $\gamma_A = \tan^{-1}\left(\frac{B}{A}\right)$.

Considering turn-off time (α_2) of SCR, the commutation must be completed within $(\pi-\gamma_A-\alpha_2)$ and $(\alpha-\pi/3-\alpha_2)$. If integral value of reverse voltage is less than $2\omega L_s I_o$, commutation failure occurs. Therefore, the commutation failure condition is expressed as:

$$\alpha \le \left(\frac{2\pi}{3}-\gamma_A\right) : \int_{\alpha}^{\alpha+\pi/3-\alpha_2} v_{ba-Adip}(t)d\omega t < 2\omega L_s I_o \tag{2.13}$$

$$\alpha > \left(\frac{2\pi}{3}-\gamma_A\right) : \int_{\alpha}^{\pi-\gamma_A-\alpha_2} v_{ba-Adip}(t)d\omega t < 2\omega L_s I_o \tag{2.14}$$

Substituting Equation (2.12) into Equation (2.13)-(2.14), and rearranging gives

$$\alpha \leq \left(\frac{2\pi}{3} - \gamma_A\right) : \sqrt{A^2+B^2}\left[\cos(\alpha+\gamma_A) - \cos\left(\alpha + \frac{\pi}{3} - \alpha_2 + \gamma_A\right)\right] < 2\omega L_s I_o \quad (2.15)$$

$$\alpha > \left(\frac{2\pi}{3} - \gamma_A\right) : \sqrt{A^2+B^2}[\cos(\alpha+\gamma_A) - \cos(\pi-\alpha_2)] < 2\omega L_s I_o \quad (2.16)$$

(2) Single phase voltage dip for B phase
If voltage dip occurs on phase B, the reverse voltage applied at T_2 is shown in Equation (2.17).

$$\begin{aligned} v_{ba-Bdip}(t) &= \sqrt{2}V_{dip}\cos\left(\omega t - \frac{\pi}{3} + \phi\right) - \sqrt{2}V_m \cos\left(\omega t + \frac{\pi}{3}\right) \\ &= \sqrt{C^2+D^2}\sin(\omega t + \gamma_B) \end{aligned} \quad (2.17)$$

where, $C = \sqrt{2}\left[V_m\frac{\sqrt{3}}{2} + V_{dip}\sin\left(\frac{\pi}{3}-\phi\right)\right]$, $D = \sqrt{2}\left[V_{dip}\cos\left(\frac{\pi}{3}-\phi\right) - \frac{V_m}{2}\right]$ and $\gamma_B = \tan^{-1}\left(\frac{D}{C}\right)$.

Similarly, we obtain Equation (2.18), (2.19).

$$\alpha \leq \left(\frac{2\pi}{3} - \gamma_B\right) : \sqrt{C^2+D^2}\left[\cos(\alpha+\gamma_B) - \cos\left(\alpha + \frac{\pi}{3} - \alpha_2 + \gamma_B\right)\right] < 2\omega L_s I_o. \quad (2.18)$$

$$\alpha > \left(\frac{2\pi}{3} - \gamma_B\right) : \sqrt{C^2+D^2}[\cos(\alpha+\gamma_B) - \cos(\pi-\alpha_2)] < 2\omega L_s I_o \quad (2.19)$$

3 Optimization Approach

3.1 Optimization for Compensation of Voltage Dip on 3-Phase PCR

Possible occurrences of commutation failure by voltage dip under specific load conditions are observed using Equations (2.10), (2.11), (2.15), (2.16), (2.18) and (2.19). Table 1 shows the parameters of PCR in facility B of A steelworks. Fig. 2 shows the relationship between voltage dip and commutation failure for the conditions shown in Table 1.

Table 1: The parameters of 3-phase PCR with B facility of A steelworks

AC input power [V]		460	Frequency [Hz]	60[Hz]
Rectifier rating	Voltage [V]	250	Overload ratio [%]	175 %
			Source Inductance (L_s) [μH]	60
	Current [A]	300	SCR turn-off time (α_2) [μs]	300

Fig. 2 shows several graphs for the possible occurrence of commutation failure depending on phase shifts, and the intensity of input voltage when firing angle is 100°, 130° and 160°. Horizontal axis is the voltage dip [%] providing voltage reduction by voltage dip divided by normal voltage. Vertical axis is phase shift of input voltage. The graphs show each areas where commutation failure is observed as a result of 3-phase parallel voltage dip and single

phase voltage dip. Statistically, voltage dip with voltage reduction ratio of below 60% (red solid line shown in Fig. 2) occupies approximately 90% of voltage dip. Normal status of input voltage would show voltage dip of 0%, and phase shift of 0°. The left side region of

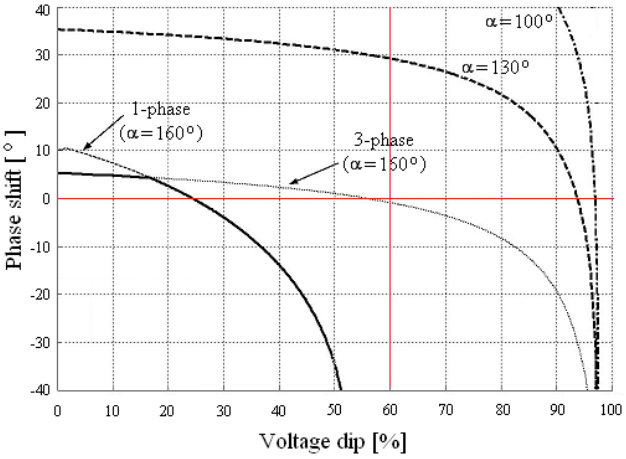

Figure 2: The permissible range of voltage dip according to the firing angle

the graph indicates the region of permissible range of voltage dip, and the right side of the graph designates the region which causes commutation failure. From Fig. 2, we can observe the range of voltage dip for various firing angles of PCR that does not cause commutation failure. We can also observe that as firing angle and phase shift of input voltage increase, even a minor change in input power can cause commutation failure. Single phase voltage dip does not cause commutation failure when firing angle is less than 130°, while it does cause commutation failure at 3-phase parallel voltage dip. When the firing angle is 160°, the left area (overlap area of 3-phase parallel voltage dip and single phase voltage dip) plotted by thick solid line does not cause commutation failure. Fig. 3 shows the permissible range of

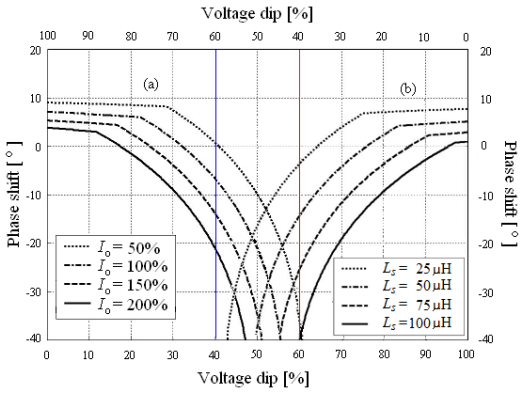

Figure 3: The permissible range of voltage dip according to the overload ratio of load current and source inductance at ($\alpha = 160°$)

voltage dip according to load current (Io) and source inductance (Ls) when the firing angle (α) for facility described in Table 1 is 160°. The plot (a) shown in Fig. 3. describes the permissible range of voltage dip for the overload ratio of load current, and plot (b) indicates data for the source inductance. From Fig. 3, we can observe the range of voltage dip that causes commutation failure at PCR for changes in load current and source inductance. As load current and source inductance increase, the permissible range of voltage dip decreases.

Fig. 4 shows the curve of commutation failure for the firing angle and voltage dip ratio at 3-phase parallel voltage dip and single phase voltage dip. In this case, we assume that the phase of line voltage is not changed by voltage dip. The right side region of each graph indicates commutation failure. It can be observed that if firing angle is greater than 130° (red solid line shown in Fig. 4), single phase voltage dip has greater effect on commutation failure than 3-phase parallel voltage dip. As shown in Fig. 5, the range of voltage dip without commutation failure increases as the maximum firing angle is limited to the small value.

Statistically, since voltage dip with voltage reduction ratio of below 60% occupies approximately total voltage dip of 90% [3, 11, 12], we can assume that if the maximum firing angle for facility described on Table 1 is limited to 143°, commutation failure would not occur. However, if the maximum value of firing angle is limited, ability to restore compensation energy produced at loading side to line voltage would decrease. Thus it requires additional systems such as dynamic breaking or chopper to prevent voltage increase in DC link caused by compensation energy.

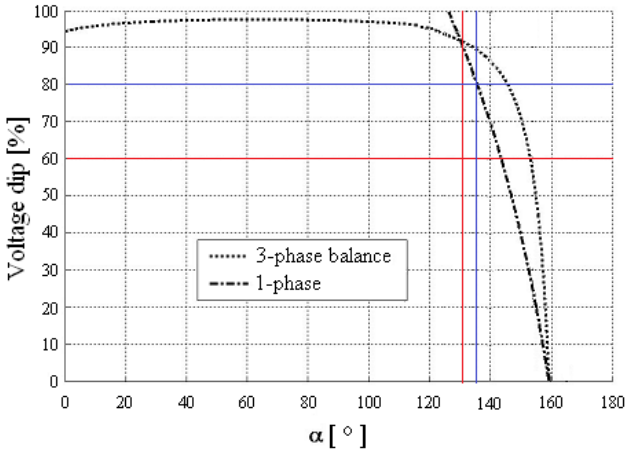

Figure 4: The curve of commutation failure for the firing angle and voltage dip when the phase is not changed

3.2 Analysis and Optimization for DVR Response Time

DVR is a device to protect load from voltage dip for the line voltage by restoring the power of load side to its original status before voltage dip does not occur. Fig. 5 shows the block diagram of DVR. As shown in Fig. 5, when the line voltage is positioned at normal state, the bypass switch is connected to directly send input power to the load side. If voltage dip occurs, bypass switch is turn-off and the reduced amount by the voltage dip is created by the inverter to be supplied to line voltage through serial transformer. This operation allows

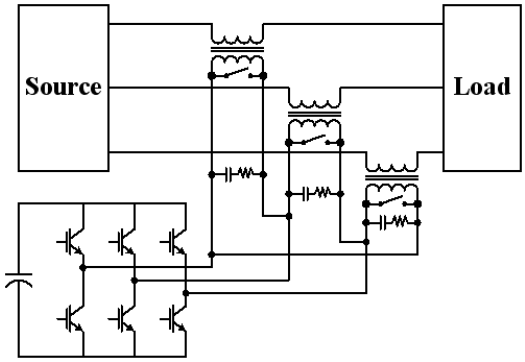

Figure 5: Block diagram of DVR

normal flow of power supply at load side even if voltage dip occurs. Thus it can effectively prevent sudden incidents from a voltage dip.

Voltage dip caused by power supply accidents such as short circuit and over current produces different voltage reductions and phase shifts depending on the distance from the site of cable accident. Therefore, DVR may not be able to completely prevent unwanted accidents. If the DVR is especially designed to protect 3-phase PCR from commutation failure caused by voltage dip, the response time of DVR is required as a very important factor to restore dropped output voltage.

Therefore, it is very important to investigate the relationship between response time of DVR and the range of compensation voltage dip. Let's consider that firing angle is larger than 120° for both 3-phase parallel voltage dip and single phase voltage dip to investigate the conditions where optimum response time is taken for commutation failure. There are several techniques to minimize the size of compensation voltage, to minimize the size of compensation energy, and to restore load voltage back to the previous state without voltage dip as compensation techniques [13]. However, the technique to minimize the size of compensation voltage and compensation energy cannot be applied for 3-phase PCR because 3-phase PCR is affected by the phase of voltage. This technique provides different voltage phases before and after the accident. Since the proposed technique provides the same voltage phases for the accidents and controls voltage dip as compensation technique using optimum response time, it has several advantages to compensate voltage dip as compared to conventional techniques.

Fig. 6 shows reverse voltage, v_{ba} at T_1 of SCR when firing angle is greater than 120°. From Fig. 6, voltage dip occurs at point α when trigger signal is sent to T_3, and compensation voltage is sent by DVR at $(\alpha + \alpha_3)$ to restore v_{ba} with normal voltage. Also, specific classification is given to the point where DVR sends compensation energy is greater than or less than the point $(\pi - \phi)$ where reverse voltage v_{ba-dip} changes its sign.

As shown in Fig. 6(a), the condition that causes commutation failure where $(\alpha + \alpha_3)$ is less than $(\pi - \phi)$ can be expressed as:

$$\int_{\alpha}^{\alpha+\alpha_3} v_{ba,dip}(t)d\omega t + \int_{\alpha+\alpha_3}^{\pi-\alpha_2} v_{ba}(t)d\omega t < 2\omega L_s I_o. \tag{3.1}$$

From Fig. 6(b), the condition that causes commutation failure where $(\alpha + \alpha_3)$ is greater

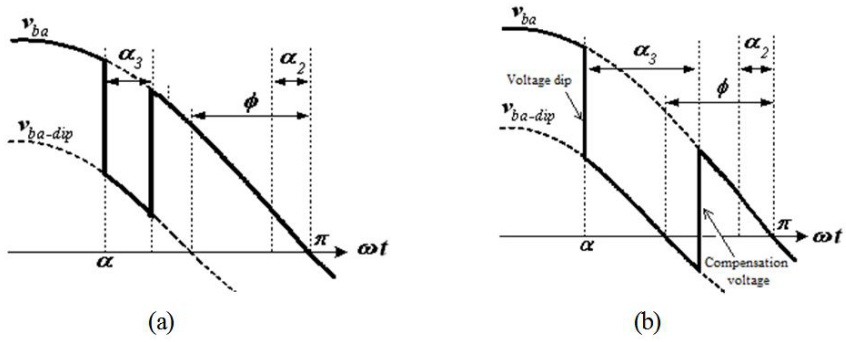

Figure 6: Voltage dip and compensation voltage: (a) $(\alpha+\alpha_3) \leq (\pi-\phi)$, (b) $(\alpha+\alpha_3) > (\pi-\phi)$

than $(\pi - \phi)$ can be expressed as:

$$\int_{\alpha}^{\pi-\phi} v_{ba,dip}(t)d\omega t < \int_{\pi-\phi}^{\alpha+\alpha_3} v_{ba,dip}(t)d\omega t. \tag{3.2}$$

In other words, if the left term of Equation (3.2) is greater than the right term of the equation, T_3 is completely turn-off before $(\alpha + \alpha_3)$, and even if DVR sends compensation energy after $(\alpha + \alpha_3)$, it is not enough to turn T_3 on, which will result in commutation failure.

Fig. 7 shows the response time of the DVR for the ranges of voltage dip, where PCR of facility described in Table 1 can be protected by the DVR. The protectable area for both single phase voltage dip and 3-phase voltage dip is presented at conditions when there is absence of the DVR, and when the DVR response time is 0.2ms, 0.3ms, and 0.4ms. The left side region of each curve is area protected by the DVR. Fig. 7(a) shows area of voltage dip protected by the DVR when the firing angle is 160°. In Fig. 7(a), if the response time is less than 0.3ms, the DVR compensates voltage dip of 60% without phase shift. Fig. 7(b) shows possible protection area when firing angle is 150°. As shown in Fig. 7(b), voltage dip of less than 60% can be compensated if the DVR response time is 0.2ms, 0.3ms, and 0.4ms, area of possible protection does not show any significant difference for various response times. Thus, when firing angle is 150° as the case in Fig. 7(b), response time of the DVR below 0.3ms is not effective. The response time of 0.3ms is only effective in the compensation for voltage dip up to voltage reduction rate of 60%.

Fig. 8 shows the range of voltage dip compensated for the firing angle and the response time of the DVR without phase shift on the facility described in Table 1. As shown in Fig. 6, commutation failure does not occur even at the absence of the DVR if firing angle is 160° and voltage reduction rate is less than 25%. Thus, if the DVR response time is more than 0.51ms from the point B of Fig. 8, there is no compensation effect. However, if the DVR response time is set as 0.28ms from point A onwards, the 3-phase PCR with maximum firing angle of 160° can be compensated for regardless of voltage reduction rate of less than 60%. Although possible compensation area can be enlarged with shorter DVR response time, it has a minor effect on the high cost of the DVR controller with a microprocessor. However, the proposed technique allows user to design DVR controller with optimum response time for low cost solution and good stability.

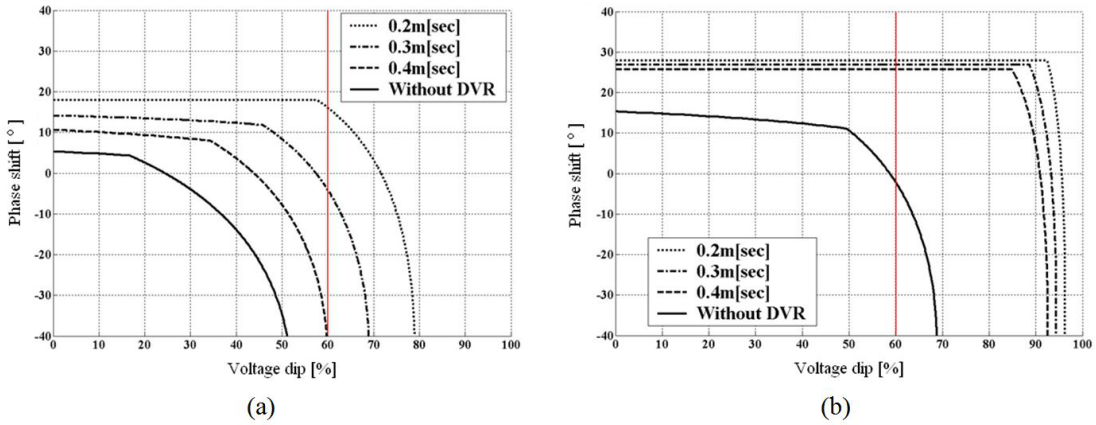

Figure 7: The range of voltage dip which can be compensated according to the response time of the DVR: (a) firing angle=160°, (b) firing angle=150°

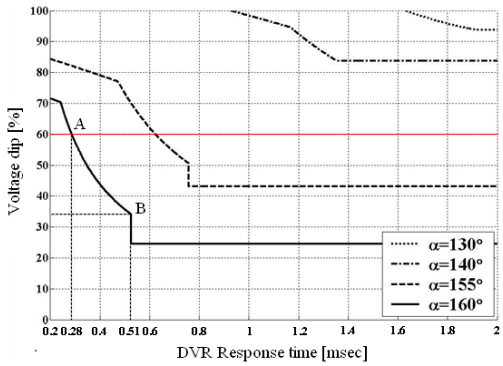

Figure 8: The range of voltage dip compensated for the firing angle and the response time of the DVR without phase shift

4 Results

To verify the proposed technique, the simulation was performed using Power System Blockset of MATLAB. As a case study, Fig. 9 shows the 3-phase line voltage from voltage dip of 80% in the A phase. The setting was done for cases where normal voltage on phase A drops by 80% from 460V to 92V without phase shift. Fig. 10 shows commutation failure for phase current and output voltage of rectifier due to voltage dip. The parameters described in Table 1 are used in simulation and firing angle is 155°. The output voltage decrease to 0[V] because of its commutation failure in SCRs D_1 and D_2.

From Fig. 4 as shown in the maximum voltage reduction rate per firing angle without commutation failure, it can be said that firing angle must be limited to 138° to prevent commutation failure when voltage dip of 80% voltage reduction rate is observed.

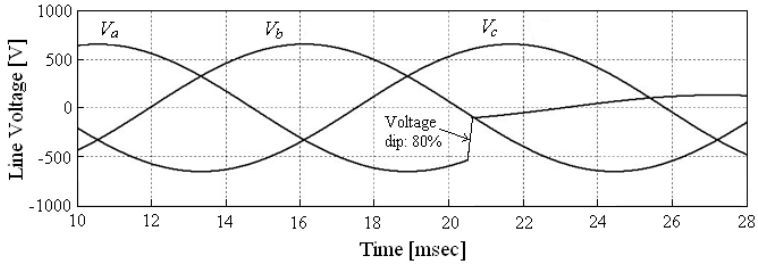

Figure 9: The 3-phase line voltage occurred from voltage dip of 80% in the A phase

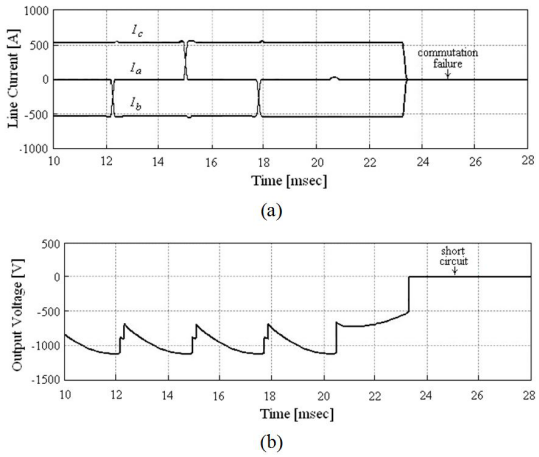

Figure 10: Waveform of PCR when firing angle is 155° (a) phase current (b) output voltage of rectifier

Fig. 11 shows the waveform of PCR when firing angle is 138° under the same conditions as Fig. 10. From Fig. 11(a) and 11(b), reduction in output voltage is observed when the commutation time is increased by reduced line voltage, but it is also clear that commutation failure does not occur under these conditions. However, if firing angle is limited from 155° to 138°, output voltage is reduced from -565V to -480V, and restoration energy created from the load cannot be effectively restored to the line voltage. Therefore, additional system is required to consume the restoration energy.

Fig. 12 and 13 show the waveform of rectifier when line voltage is compensated by the DVR. The condition contains firing angle of 155°, single phase voltage dip of 80% voltage reduction rate, and it also contains the parameters described in Table 1. Let's assume that once voltage dip occurs, the DVR restores the voltage and phase of line input voltage back to its original state. As already shown in Fig. 8, the range of voltage dip can be compensated for the maximum response time of 352μs in the DVR. This maximum response time of the DVR can protect the rectifier when firing angle is 155°, and voltage reduction rate is 80%.

Fig. 12 shows the waveform of PCR when the DVR response time is 352μs. Fig. 12(a) represents the waveform of line voltage compensated by the DVR. It also shows the reduction of line voltage at phase A by the voltage dip, and its restoration state by the DVR after

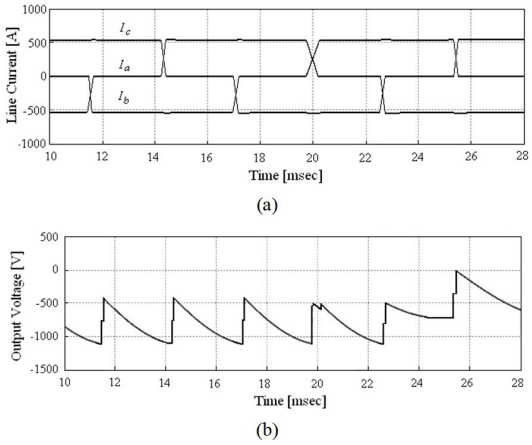

Figure 11: Waveform of PCR when firing angle is 138° (a) phase current (b) output voltage of rectifier

352μs. Fig. 12(b) shows the phase current of rectifier. It was set to cause voltage dip as soon as trigger signal is sent to SCR T_3, so commutation does not conducted between phase A and phase B when the voltage dip occurs. However, commutation conducted successfully as soon as line voltage is compensated after DVR response time. Output waveform of PCR is shown in Fig. 12(c), and it shows that the DVR effectively restores voltage dip for normal operation of rectifier.

Fig. 13 depicts the waveform for the response time of 352μs in the DVR. The voltage dip at line voltage, and restoration of normal state by the DVR after 352μs can be observed in Fig. 13(a). Fig. 13(b) shows commutation failure from about 23.4ms. When the next trigger signal is sent in Fig. 13(c), output voltage indicates at 0V providing short circuit. Therefore it can be observed that setting the DVR response time of less than 352μs can protect the facility described in Table 1 from all voltage dips with voltage reduction rate of up to 80%. However, the proposed technique can be used to obtain the relationship between the DVR response time and permissible range of compensated voltage dip. It is helpful to design optimum 3-phase PCR.

5 Conclusion

In this paper, we presented optimization technique and analytical analysis for the response time of DVR. It was analyzed by the relationship between possible compensation range of voltage dip, and the response time of DVR as an important design factor to protect 3-phase phase-controlled rectifier from voltage dip. We also investigated the possible compensation range of voltage dip by the DVR system using proposed technique for the optimum response time. This paper proposed optimum response time required for certain intensity of voltage dips for the DVR system, and good stability to support possible compensation range of voltage dip. Proposed technique showed optimum response time and good stability for overall system. We believe that proposed technique is reliable and useful in DVR design.

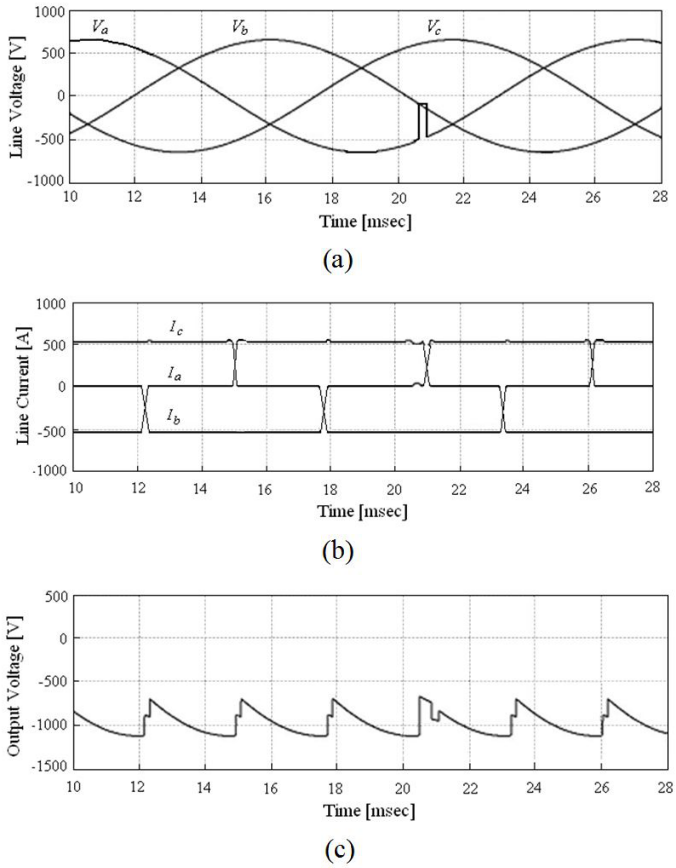

Figure 12: Waveform of phase-controlled rectifier for the response time of 352μs in the DVR (a) compensated line voltage (b) phase current (c) output voltage

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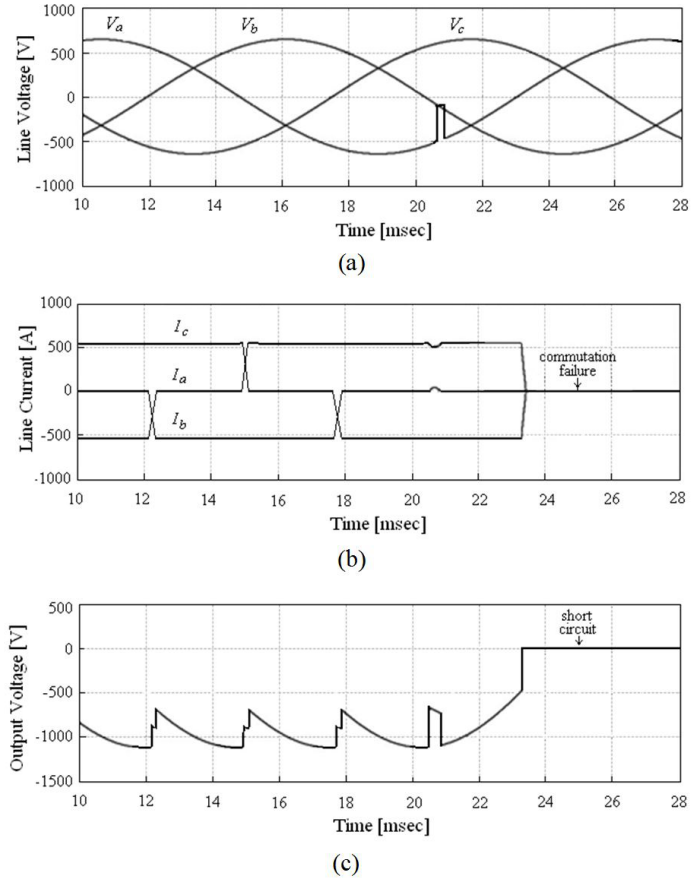

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